subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

By _____
Michael E. Marion, Reg. 32,266
Attorney
(914) 333-9641

APPENDIX

3. (Amended) The filter (3) according to claim 1 ~~or 2~~, characterised in that the filter (3) is provided with control means (Contr.) coupled to FET capacitor control inputs (G1-32; G'1-32).

4. (Amended) The filter (3) according to ~~one of the~~ claims ~~1-3~~, characterised in that the FET capacitors (M1-32; M'1-32) are split in equally controlled pairs of FET capacitors (M1-32; M'1-32).

5. (Amended) The filter (3) according to ~~one of the~~ claims ~~1-4~~, characterised in that the filter (3) is built up as a symmetrically filter (3) having a symmetrical input (5) and a symmetrical output (6).

6. (Amended) The filter (3) according to ~~one of the~~ claims ~~1-5~~, characterised in that two or more of the FET capacitors (M1-32; M'1-32) are connected in series.

7. (Amended) The filter (3) according to ~~one of the~~ claims ~~1-6~~, characterised in that the FET capacitors ()M1-32; M'1-32 are metal oxide semiconductor (MOSFET) capacitors (M1-32; M'1-32).

8. (Amended) A transmitter, receiver, or transceiver having a filter (3) according to ~~one of the~~ claims ~~1-7~~, which filter (3) is provided with field effect (FET) capacitors (M1-32; M'1-32) arranged for controlling their respective capacity values, each such FET capacitor (M1-32; M'1-32) having a source (S) and a drain (D), characterised in that the source (S) and the drain (D) of each FET capacitor (M1-32; M'1-32) are coupled to one another.